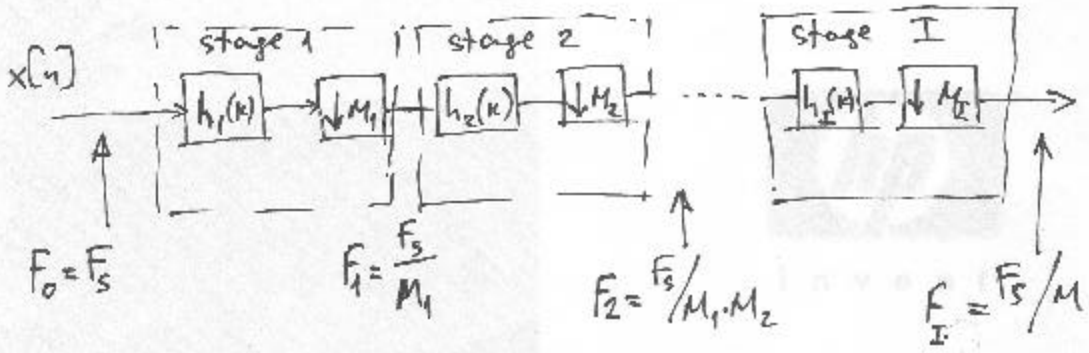
Multistage implementation of digital filters and sampling rate conversion.

When large changes in the sampling rate are required it is often more efficient to change the rate in more than one steps (stages). This leads to significant reduction in the requirements of the anti-aliasing or anti-imaging filter and an overal reduction in computational requirements

In the next figure an I-stage decimation process is shown where the overall decimation factor is $M = M_1 \cdot M_2 \cdots M_I$

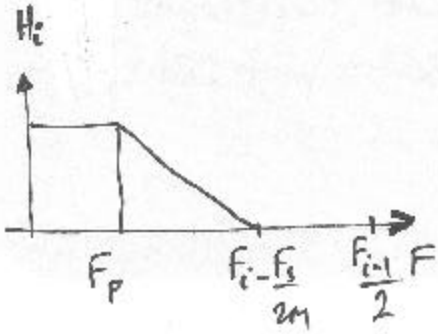


Assuming a single stage implementation, then, $x[n]$ must be bandlimited to $\frac{F_s}{2M}$ to avoid aliasing that is the filter must have the following characteristics

	Real Frequencies	Normalized frequencies
passband:	$0 \le F \le F_p$	$0 \le w \le \frac{2\pi F_p}{F_s}$
stopband:	$\frac{F_s}{2M} \le F \le F_s/2$	$\frac{\pi}{M} \le w \le \pi$

Assuming now a multistage implementation, then, the following "tolerance" scheme can be derived for

(stage i) Filter i



	Real freq.	Normalized freq
passband:	$0 \le F \le F_p$	$0 \le \omega \le \frac{2\pi F_p}{F_{i-1}}$
stopband:	$F_i - \frac{F_s}{2M} < F < \frac{F_{i-1}}{2}$	$\frac{2\pi}{F_{i-1}}\left(F_i - \frac{F_s}{2M}\right) < \omega < \pi$

(Notice that Filter i operates at rate F_{i-1})

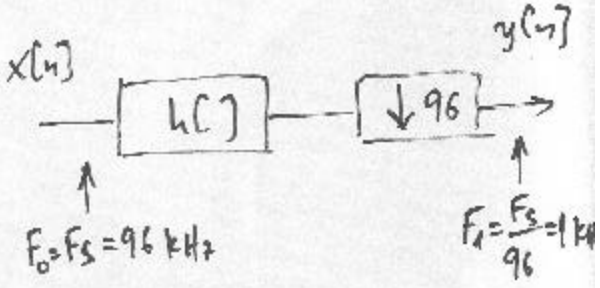
Looking at this "tolerance" scheme we can make the following observation

* Any aliasing in frequency will be restricted in the range between $\frac{F_s}{2M} < F < F_i - \frac{F_s}{2M}$ and therefore it will be eventually filtered out.

Thus, by allowing aliasing to occur in intermediate stages the design of intermediate filters is relaxed and this ends up to a more efficient implementation overall:

Ex: We want to design a filter + decimation with the following specifications

Passband: $F_p = 450$ Hz
Stopband: $F_{st} = 500$ Hz
Sampling Freq.: $F_s = 96$ kHz



Let us consider a multistage (3-stage implementation) of the decimator where $96 = M = M_1 \cdot M_2 \cdot M_3 = 8 \cdot 6 \cdot 2$

So according to the Figure $F_0 = F_s = 96$ KHz

$$F_1 = \frac{F_s}{M_1} = 12 \text{ KHz}$$

$$F_2 = \frac{F_s}{M_1 \cdot M_2} = 2 \text{ KHz}$$

$$F_3 = \frac{F_s}{M} = 1 \text{ KHz}$$

The following table can be constructed:

	F_{i-1}	$w_p = \frac{2\pi F_p}{F_{i-1}} = \frac{2\pi \cdot 0.45}{F_{i-1}}$	$w_{st} = \frac{2\pi}{F_{i-1}}\left(F_i - \frac{F_s}{2M}\right)$	$w_s - w_p$	# of coefficients of FIR Filter assuming rectangular window in the design $M = \frac{4\pi}{w_{st} + w_p}$
H_1	96 kHz	$0.0094\,\pi$	$0.2396\,\pi$	$0.2302\,\pi$	$M = 9$
H_2	12 kHz	$0.0750\,\pi$	$0.2500\,\pi$	$0.1750\,\pi$	$M = 12$
H_3	2 kHz	$0.4500\,\pi$	$0.5\,\pi$	$0.05\,\pi$	$M = 40$

Comparing to a single stage implementation where

$$w_p = \frac{2\pi 450}{96 \cdot 10^3} = \frac{0.9\,\pi}{96}, \quad w_{st} = \frac{2\pi 500}{96 \cdot 10^3} = \frac{\pi}{96}, \quad \Delta w = w_{st} - w_p = \frac{0.1\pi}{96}$$

then an FIR filter of length $M \simeq \frac{4\pi \cdot 96}{0.1\pi} = 3,840$ (rectangular window based design) coefficients is needed.

Obviously the total number of coefficients as well as the corresponding # of computations/sec are significantly less for the multistage implementation.