FINAL EXAMINATION
ECE431H1F, Digital Signal Processing

December 14, 2012
Examiner: D. Hatzinakos

Time: 9:30 am-12:00 noon, Room WB219

1. This is a closed book exam (Type A)
2. Non-programmable calculators are allowed.
3. Please solve all five problems. All problems are equally weighted,
4. All answers must be written in the examination booklet. Do not write any answers in this problem handout.

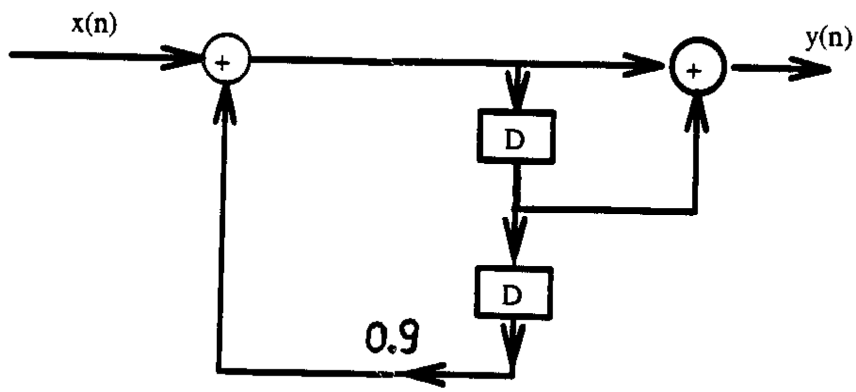
PROBLEM 1 (20 points)
Please answer the following questions. All questins are equally weighted -2 points

1. If a continuous –time signal is sampled and the sample values are applied in a digital computer, why is the sample value used in the computer generally not equal to the value of the continuous-time signal at the sampling instant?
2. Explain why a discrete time signal formed by sampling a periodic continuous-time signal may not be periodic. What are the conditions required for the discrete-time signal to be periodic?
3. Explain the importance of zero padding for FFT calculations.
4. Explain the importance of knowing the region of convergence (ROC) for Z-transforms.
5. You are asked to design a low pass filter that has 70 dB attenuation in the stop-band. How many bits are needed in the A/D (Analog to Digital converter)?
6. What is the purpose of an oversampling filter in a CD player and why is it used? If there were no oversampling filter, what alternative would the designer have to achieve the same quality on the output?
7. A sinusoid at 400 Hz is sampled at 5,000 Hz. If the sinusoid is down-sampled by a factor of 10 by removing 9 samples out of each set of 10, the frequency of the down-sampled sinusoid will be 100 Hz. Explain.
8. When we up-sample (interpolate) a signal, we do so by first inserting zeros between the existing samples and follow with a low-pass filter which "fills in" the zeroed sample points. Are we creating new information? If so, does it accurately reflect the true value of the signal? Is there any difference between, say, sampling a signal which is band –limited to 0Hz to 100 Hz at 1 KHz and sampling the same signal at 500 Hz and use an interpolator to up-sample it to 1KHz?
9. Construct a mathematical argument to show that IIR filters are more sensitive to quantization noise than their FIR counterparts.
10. A linear phase FIR filter has 6 zeros. Two of the zeros are at locations, $z1=0.5-j0.5$ and $z2= 1/3$. What are the locations of the remaining 4 zeros?

DO NOT WRITE IN THIS SPACE

PROBLEM 2 (10 points)

Consider the linear time invariant discrete-time filter of the figure:



1. Write the Linear Constant Coefficient Difference Equation (LCCDE) that describes the system (D denotes unit delay).
2. Calculate the Discrete-time Fourier Transform (DTFT) of the system impulse response. Sketch approximately the DTFT.
3. Provide a cascade realization of the filter in terms of two sections and provide an analysis of fixed point arithmetic effects in the output of the filter.

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PROBLEM 3 (10 points)

We have a discrete-time signal x[n], arriving from a source at a rate of 1/T1 samples /sec.. We want to digitally resample it to create a signal y[n] that has 1/T2 sample/sec , where T2=3/5 T1.

a) Draw a block diagram of a system to perform the re-sampling. Specify, the input/output relationship for all the boxes in the Fourier domain.
b) For an input signal

$$x[n] = \delta[n] = \begin{cases} 1, & n = 0 \\ 0, & \textit{otherwise} \end{cases}$$

determine y[n].

DO NOT WRITE IN THIS SPACE

PROBLEM 4 (10 points)
You are given a number of 4-point FFT chips and you are asked to choose N and perform an N-point DFT of a sequence of length 11 samples , that is, $x(n)$, $n=0,1,\ldots, 10$. How many chips will you interconnect in order to achieve minimum number of multiplications? Show explicitly how you should interconnect these chips to compute the N-point DFT (include diagram and expressions). What is the number of multiplications and additions required?

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